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Serial I/O Driver for Microsoft Windows* 10 64-bit OS on Intel Atom® x6000E Series, and Intel Pentium® and Celeron® N and J Series Processors (Code Name: Elkhart Lake)

Release Note

August 2021

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Revision History

Date	Revision	Description
August 2021	1.2	MR1 Release
April 2021	1.1	Added support to Embedded SKU
March 2021	1.0	PV Release for PC Client and Industrial Non-FuSa SKU
January 2021	0.9	Pre-production QS Release
October 2020	0.8	Beta 3 Engineering Release
September 2020	0.7	Beta Release
July 2020	0.6	Alpha 2 Release
May 2020	0.5	Alpha Release
April 2020	0.3.1	Engineering Release #2
November 2019	0.3	Initial release

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1.0   Introduction

This release note provides information on driver interfaces, limitations, and known issues for the serial I/O driver binary packages for the Microsoft Windows* 10 64-bit operating system.

1.1   Acronyms and Terminology

Table 1.   Terminology

Term	Description
BKC	Best-Known Configuration
BKM	Best-Known Method
DMA	Direct Memory Access
GPIO	General-Purpose I/O
HS-UART	High-Speed Universal Asynchronous Receiver/Transmitter
IOCTL	I/O Control
ODM	Original Design Manufacturing
OEM	Original Equipment Manufacturing
PIO	Programmed I/O
SoC	System on a Chip
SPB	Simple Peripheral Bus
UART	Universal Asynchronous Receiver/Transmitter

1.2   Intended Audience

This document is intended for OEMs and ODMs that are enabling drivers with the Intel Atom® x6000E Series, Intel® Pentium® and Celeron® N and J Series processors.

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1.3 Customer Support

Contact your Intel representative for support or submit an issue to Intel® Premier Support:

http://premiersupport.intel.com.

1.4 Reference Documents

Log in to the Resource and Design Center (www.rdc.intel.com) to search for and download the document numbers listed in the following table. Contact your Intel field representative for access.

Note: Third-party links are provided as a reference only. Intel does not control or audit third-party benchmark data or the web sites referenced in this document. You should visit the referenced web site and confirm whether the referenced data are accurate.

Table 2. Reference Documents

Document	Document No./Location
Best-Known Configuration (BKC) for Microsoft Windows* 10 RS5 (64-bit) OS on Intel Atom® x6000E Series Processors, Intel® Pentium® and Celeron® N and J Series Processors (Code name: Elkhart Lake)	616386

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2.0   Release Summary

2.1   Hardware and Software Compatibility

This release is compatible with the following hardware:

- Intel Atom® x6000E Series, Intel® Pentium® and Celeron® N and J Series Processors

This release supports the following operating system:

- Microsoft Windows* 10 64-bit RS5 operating system

2.2   Release Contents

This release includes the following:

- Serial I/O driver installer for Microsoft Windows* 10 64-bit operating system.
    - GPIO host controller driver (iaLPSS2_GPIO2) version 5.123.1.1023
    - I2C* host controller driver (iaLPSS2_I2C) version 5.123.1.1023
    - SPI host controller driver (iaLPSS2_SPI) version 5.123.1.1023
    - UART host controller driver (iaLPSS2_UART2) version 5.123.1.1023
    - UART host controller sub-device driver (UartSubDevice) version 5.123.1.1023

- Serial I/O drivers release notes for Microsoft Windows* 10 operating system

- Intel Software License Agreement

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3.0 Feature Highlights and Limitations

3.1 GPIO Host Controller Driver

Refer to the following link for details about the GPIO framework extension (GpioClx): https://msdn.microsoft.com/en-us/library/windows/hardware/hh439456(v=vs.85).aspx

The driver binary package consists of the following files:

- iaLPSS2_GPIO2.inf
- iaLPSS2_GPIO2.cat
- iaLPSS2_GPIO2.sys

Enabled features are as follows:

- Supports GPIO direction setting: configures the selected GPIO pin as an input or output pin
- Supports GPIO read pin: reads the input pin's level value
- Supports GPIO write pin: configures an output pin's level as high or low
- Supports GpioClx DDI.

Limitation(s) are as follows:

- Multiplexing - Any pin-multiplexing and pad configuration must be completed in the firmware prior to handing control to the OS loader.

3.2 I2C* Host Controller Driver

Refer to the following link for details on the I2C* SPB controller driver: https://docs.microsoft.com/en-us/windows-hardware/drivers/spb/spb-controller-drivers

There are seven I2C* controllers on Intel Atom® E3000 Processor, Intel® Celeron® Processor N2XXX and Intel® Celeron® Processor J1XXX sharing same DMA engine. Hence, transferring a big data size will caused one I2C* controller to occupy the DMA engine for a long duration.

The application can use multiple single transfers or IOCTL_I2C_EXECUTE_SEQUENCE interface to transfer big data.

By default, the I2C* driver uses the DMA to copy data between peripheral and system memory but can set windows registry to disable the DMA feature and copy data by PIO mode. Refer to the BKM section on how to set the registry.

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The driver binary package consists of the following files:

- iaLPSS2_I2C.inf
- iaLPSS2_I2C.cat
- iaLPSS2_I2C.sys

Enabled features are as follows:

- Supports 7-bit address mode

- Supports standard mode (100 Kbps), fast mode (400 Kbps), fast mode plus (1 Mbps), and high-speed mode (3.4 Mbps)

- Supports DMA and PIO transfer modes

- Operates only on the primary mode

- Support polling of IO data transfer

Limitation(s) are as follows:

- 10-bit address mode

- The maximum single transfer size is limited to 64Kbytes. Multiple transfers are required for data size of more than 64KB

3.3   SPI Host Controller Driver

Refer to the following link for details on the SPI SPB controller driver: https://docs.microsoft.com/en-us/windows-hardware/drivers/spb/spb-controller-drivers

The driver binary package consists of the following files:

- iaLPSS2_SPI.inf
- iaLPSS2_SPI.cat
- iaLPSS2_SPI.sys

Enabled features are as follows:

- Supports SPI modes 0, 1, 2, and 3

- Supports data bit length of 4 to 32

- Supports transfer rate at the minimum of 100 Kbps and at maximum rate 15 Mbps

- Supports DMA and PIO transfer modes

- Operates only on the primary mode

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- Supports polling of IO data transfer (Read/Write)

Limitation(s) are as follows:

- No known limitation

3.4   UART Host Controller Driver

Refer to the following link for details on the SerCx2 framework:
https://msdn.microsoft.com/en-us/library/windows/hardware/hh439599(v=vs.85).aspx

The driver binary package consists of the following files:

- iaLPSS2_UART2.inf
- iaLPSS2_UART2.cat
- iaLPSS2_UART2.sys

Enabled features are as follows:

- Supports baud rates up to 4 M

- Supports data sizes of 5, 6, 7, and 8 bits

- Supports none, odd, and even parities

- Supports 1, 1.5, and 2 stop bits

- Supports "Hardware" and "None" flow controls

- Supports full-duplex transmission and reception of data

- Supports DMA and PIO transfer modes

- Supports Serial.sys and SerCx2 (**Note:** Serial.sys supports both None and Hardware Flow control, SerCx2 only supports Hardware Flow control)

Limitation(s) are as follows:

- When using 1.5 stop bits, the data size can only be supported up to 5-bits

- The following are IOCTLs that are not supported in the driver:
    - `IOCTL_SERIAL_XOFF_COUNTER`
    - `IOCTL_SERIAL_LSRMST_INSERT`
    - `IOCTL_SERIAL_SET_BREAK_ON`
    - `IOCTL_SERIAL_SET_BREAK_OFF`

- Not supported on Y and Z modem data transfer

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3.5   UART Host Controller Sub-Device Driver

Refer to the following link for details on the SerCx2 framework: https://msdn.microsoft.com/en-us/library/windows/hardware/hh439599(v=vs.85).aspx

The driver binary package consists of the following files:

- uartsubdevice.inf
- uartsubdevice.cat
- uartsubdevice.sys

Enabled features are as follows:

- Supports serial I/O interface to perform data transfer via serial terminal

3.6   Known Issues – Open

Refer to the "Best-Known Configuration (BKC) for Microsoft Windows* 10 RS5 (64-bit) OS on Intel Atom® x6000E Series Processors, Intel® Pentium® and Celeron® N and J Series Processors" (Document Number: 616386) for known issues.

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4.0 *Guide*

4.1 Driver Installation

1. Follow these steps to install GPIO, I2C, SPI, HS-UART driver package:

    a. Extract and locate "iaLPSS2_UART2.inf." Right-click and select **install**.

    b. For SPI "iaLPSS2_SPI.inf," right-click and select **install**.

    c. For GPIO "iaLPSS2_ GPIO2 .inf," right-click and select **install**.

    d. For I2C "iaLPSS2_ I2C.inf," right-click and select **install**.

    e. Restart the system after installation has been completed.

2. Follow these steps to install HS-UART Sub Device Driver:

    a. Locate "UartSubDevice.inf." Right-click and select **install**.

    b. Restart the system after installation has been completed.

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5.0   Software BKM

5.1   What is the Baud Rate of HS-UART and How to Set It

Default baud rate is configured to 115200. Any other baud rate setting is done through the application.

5.2   Enable the UART driver to use Serial.sys/SerCx2 Framework

The UART driver can be made to use Serial.sys or SerCX2 framework by editing the below registry key.

HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\iaLPSS2_UART2\Parameters:

`Framework = 1`; default, to enable driver to use `SerCX2 framework`

`Framework = 0`; to enable driver to use legacy `Serial.sys`.

5.3   Enable the PIO or DMA feature of HS-UART

The DMA feature is switched using the following registry entry:

HKEY_LOCAL_MACHINE\SYSTEM\CurrentControlSet\Services\iaLPSS2_UART2\Parameters:

`ForcePIOMode = 0`; default, to enable `HS-UART DMA` feature;

`ForcePIOMode = 1`; to enable `HS-UART PIO` feature.

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